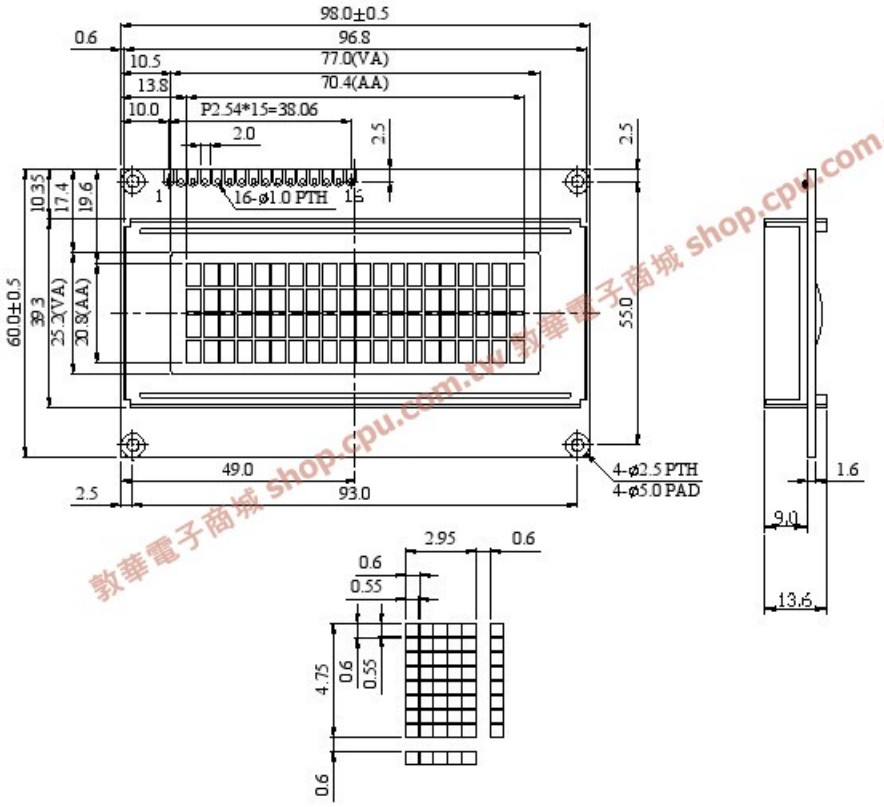
2.Dimension Drawing



3. Precaution in use of LCD Display Module

3.1Use Modules

1. When modules switch on or off, after accessing positive supply power with 5±0.5 voltage ,then input signal levels, if signal levels input before supply power becomes stable or switches off, IC circuits off, modules will be damaged , as a result , modules will be damaged.
2. Dot matrix modules are high path –number LCDs, they are largely related to the contrast ,view angle ,driving voltage when displaying , so you should adjust it to get best contrast and view angle, if it is too high , not only displays are effected, but also let life shorted.
3. When using under regulated working temperature below, the display responsiveness it too slow, when using under regulated temperature above, whole display surface turns dark, this is not damaged, when the temperature returns normal, all displays become normal

3.2Module storage

1. Storaging temperature:-30~+80℃
2. Place in dark sites to avoid strong lights
3. Don't place other thing on their surfaces
4. Packaged in polyer materials (with anti-static electricity layers) and sealed

4. General Features

(1) Mechanical Dimension

Item	Dimension	Unit
Number of Characters	20characters x 4 Lines	—
Module dimension (L x W x H)	98.0 x 60.0 x 13.6 (Max)	mm
View area	77.0 x 25.2	mm
Active area	70.4 x 20.8	mm
Dot size	0.55 x 0.55	mm
Dot pitch	0.6 x 0.6	mm
Character size (L x W)	2.95 x 4.75	mm
Character pitch (L x W)	3.55 x 5.35	mm

(2) Controller IC: **ST7066U-OA**

(4)LCD:STN,Y/G ,6H view ,Positive Type

5. Electrical Maximum Ratings

5.1 Electrical Absolute Maximum Ratings

(Vss=0V, Ta=25℃)

Item	Symbol	Min	Max	Unit
Supply Voltage (Logic)	Vdd-Vss	-0.3	7	V
Supply Voltage (LCD driver)	Vdd-Vo	-0.3	13	V
Input Voltage	VI	Vss	Vdd	V
Wide Temperature Type	Top	-20	+70	℃
	Tstg	-30	+80	℃

6. Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	Vdd-Vss	—	3.0	4.0	5.5	V
Supply Voltage For LCD ＊Wide Temp、Type	Vdd-Vo	Ta=-20℃	—	5.0	—	V
		Ta=0℃	—	4.5	—	V
		Ta=25℃	3.7	**4.2**	4.3	V
		Ta=50℃	—	4.0	—	V
		Ta=+70℃	—	3.5	—	V
Input High Volt.	V_{IH}	—	2.2	—	Vdd	V
Input Low Volt.	V_{IL}	—	—	—	0.6	V
Output High Volt.	V_{OH}	—	2.4	—	—	V
Output Low Volt.	V_{OL}	—	—	—	0.4	V
Supply Current (LCM)	Idd	Vdd=5V	—	1.5	—	mA
Supply Current LED B/L	ILED	VLED=4.2V	—	250		mA

7. Optical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
View Angle	Top			75		deg
	Down			30		deg
	Right			+30		deg
	Left			-30		deg
Contrast Ratio	CR	—		4		—
Response Time	T rise	25℃		100		us
	T fall	25℃		150		us

8. Backlight

8.1 Electrical Ratings

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Forward voltage	V_F	I_F=250mA	4.0	4.2	4.3	V
Reverse current	I_R	V_R=8V	-	-	1	mA
Luminous intensity	I_V	I_F=250mA		100	-	cd/m^2
Wavelength	λp	-		575		nm
Color	Y/G					

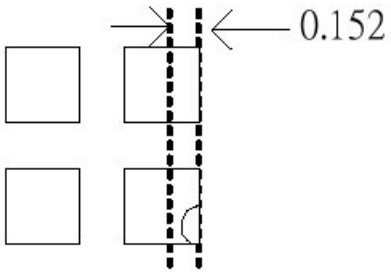
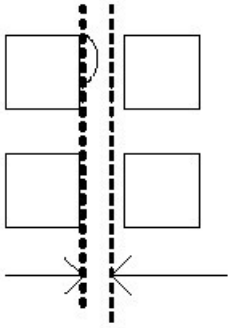
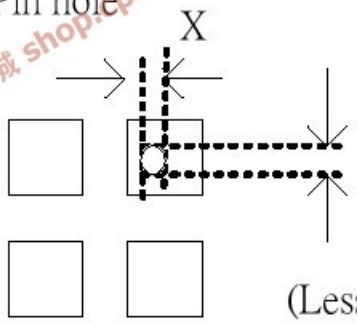
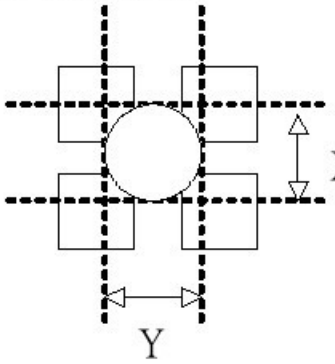
Input 4.2V/250mA on Pin(15) Pin(16)

9. Interface Pin Function

Pin No.	Symbol	Level	Description
1	Vss	0V	Supply Voltage for logic **GND**
2	Vdd	5V	Supply Voltage for logic
3	Vo	4.2V	VDD-Vo Contrast adjust
4	RS	H/L	H:DATA, L:Instruction code
5	R/W	H/L	H:Read(MPU→Module)L:Write(MPU→Module)
6	E	H,H→L	Chip enable signal
7	DB0	H/L	Data bit 0
8	DB1	H/L	Data bit 1
9	DB2	H/L	Data bit 2
10	DB3	H/L	Data bit 3
11	DB4	H/L	Data bit 4
12	DB5	H/L	Data bit 5
13	DB6	H/L	Data bit 6
14	DB7	H/L	Data bit 7
15	A	4.2V	LED Backlight V+
16	K	0V	LED Backlight V-

10.Quality Assurance

<table>
<tr><th>NO.</th><th>Parameter</th><th>Criteria</th></tr>
<tr><td>1</td><td>Black or White spots</td><td>
<table>
<tr><th rowspan="2">Zone
Dimension</th><th colspan="2">Acceptable Number</th><th rowspan="2">Class Of Defects</th><th rowspan="2">Acceptable Level</th></tr>
<tr><th>A</th><th>B</th></tr>
<tr><td>D＜0.15</td><td>*</td><td>*</td><td rowspan="4">Minor</td><td rowspan="4">2.5</td></tr>
<tr><td>0.15≦D≦0.2</td><td>4</td><td>4</td></tr>
<tr><td>0.2≦D≦0.25</td><td>2</td><td>2</td></tr>
<tr><td>D≦0.3</td><td>0</td><td>1</td></tr>
</table>
D=(Long + Short)/2 *: Disregard
</td></tr>
<tr><td>2</td><td>Scratch, Substances</td><td>
<table>
<tr><th colspan="2" rowspan="2">Zone
X(mm) Y(mm)</th><th colspan="2">Acceptable Number</th><th rowspan="2">Class Of Defects</th><th rowspan="2">Acceptable Level</th></tr>
<tr><th>A</th><th>B</th></tr>
<tr><td>*</td><td>0.04≧W</td><td>*</td><td>*</td><td rowspan="4">Minor</td><td rowspan="4">2.5</td></tr>
<tr><td>3.0≧L</td><td>0.06≧W</td><td>4</td><td>4</td></tr>
<tr><td>2.0≧L</td><td>0.08≧W</td><td>2</td><td>3</td></tr>
<tr><td>—</td><td>0.1＜W</td><td>0</td><td>1</td></tr>
</table>
X: Length Y: Width *: Disregard
Total defects should not exceed 4/module
</td></tr>
<tr><td>3</td><td>Air Bubbles (between glass & polarizer)</td><td>
<table>
<tr><th rowspan="2">Zone
Dimension</th><th colspan="2">Acceptable Number</th><th rowspan="2">Class Of Defects</th><th rowspan="2">Acceptable Level</th></tr>
<tr><th>A</th><th>B</th></tr>
<tr><td>D≦0.15</td><td>*</td><td>*</td><td rowspan="3">Minor</td><td rowspan="3">2.5</td></tr>
<tr><td>0.15＜D≦0.25</td><td>2</td><td>*</td></tr>
<tr><td>0.25＜D</td><td>0</td><td>1</td></tr>
</table>
*: Disregard
Total defects shall not excess 3/module.
</td></tr>
</table>

4	Uniformity	(1) Pixel shape (with Dent)  (2) Pixel shape (With Projection)  (3) Pin hole  (Less than 0.1mm is no counted) (4)Deformation  Total acceptable number : 1/pixel,5/cell

11. Reliability

■Content of Reliability Test

Environmental Test				
No.	Test Item	Content of Test	Test Condition	Display
1	High Temperature storage	Endurance test applying the high storage temperature for a long time.	70℃ 200hrs	No damage
2	Low Temperature storage	Endurance test applying the high storage temperature for a long time.	-20℃ 200hrs	No damage
3	High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	50℃ 200hrs	No damage
4	Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	0℃ 200hrs	No damage
5	High Temperature/ Humidity Storage	Endurance test applying the high temperature and high humidity storage for a long time.	50℃,90%RH 96hrs	No damage
6	High Temperature/ Humidity Operation	Endurance test applying the electric stress (Voltage & Current) and temperature / humidity stress to the element for a long time.	40℃,90%RH 96hrs	No damage
7	Temperature Cycle	Endurance test applying the low and high temperature cycle. -10℃ 25℃ 50℃ 30min 5min 30min 1 cycle	-10℃/50℃ 10 cycles	No damage
Mechanical Test				
8	Vibration test	Endurance test applying the vibration during transportation and using.	10~22Hz→1.5mmp-p 22~500Hz→1.5G Total 0.5hrs	No damage
9	Shock test	Constructional and mechanical endurance test applying the shock during transportation.	50G Half sign wave 11 msedc 3 times of each direction	No damage
10	Atmospheric pressure test	Endurance test applying the atmospheric pressure during transportation by air.	115mbar 40hrs	No damage
Others				
11	Static electricity test	Endurance test applying the electric stress to display surface	VS=2kV 1 time	No damage

***Supply voltage for logic system=5V.

12.Controller data (ST7066)

※ Function description (Compatible with LCD controller HD44780)

The LCD display Module is built in a LSI controller, the controller has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as display clear and cursor shift, and address information for display data RAM (DDRAM) and character generator (CGRAM). The IR can only be written from the MPU. The DR temporarily stores data to be written or read from DDRAM or CGRAM. When address information is written into the IR, then data is stored into the DR from DDRAM or CGRAM. By the register selector (RS) signal, these two registers can be selected.

RS	R/W	Operation
0	0	IR write as an internal operation (display clear, etc.)
0	1	Read busy flag (DB7) and address counter (DB0 to DB7)
1	0	Write data to DDRAM or CGRAM (DR to DDRAM or CGRAM)
1	1	Read data from DDRAM or CGRAM (DDRAM or CGRAM to DR)

Busy Flag (BF)

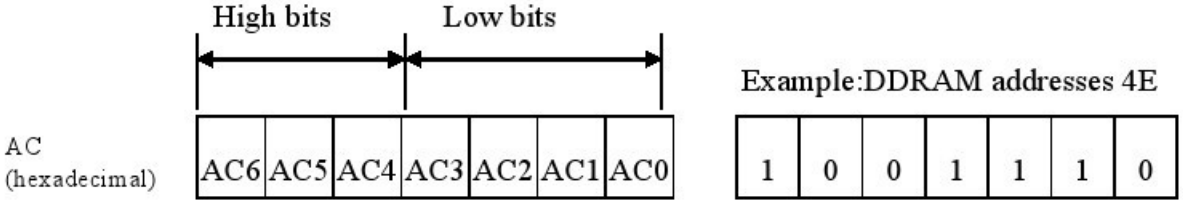
When the busy flag is 1, the controller LSI is in the internal operation mode, and the next instruction will not be accepted. When RS=0 and R/W=1, the busy flag is output to DB7. The next instruction must be written after ensuring that the busy flag is 0.

Address Counter (AC)

The address counter (AC) assigns addresses to both DDRAM and CGRAM

Display Data RAM (DDRAM)

This DDRAM is used to store the display data represented in 8-bit character codes. Its extended capacity is 80×8 bits or 80 characters. Below figure is the relationship between DDRAM addresses and positions on the liquid crystal display.



* DDRAM Address

Display position DDRAM address

1	2	3	4	5	6	----	-----	----	----	----	20
00	01	02	03	04	05						13
40	41	42	43	44	45						53
14	15	16									27
54	55	56									67

20 Character * 4 Line

Character Generator ROM (CGROM)

The CGROM generate 5×8 dot or 5×10 dot character patterns from 8-bit character codes. See Table 2.

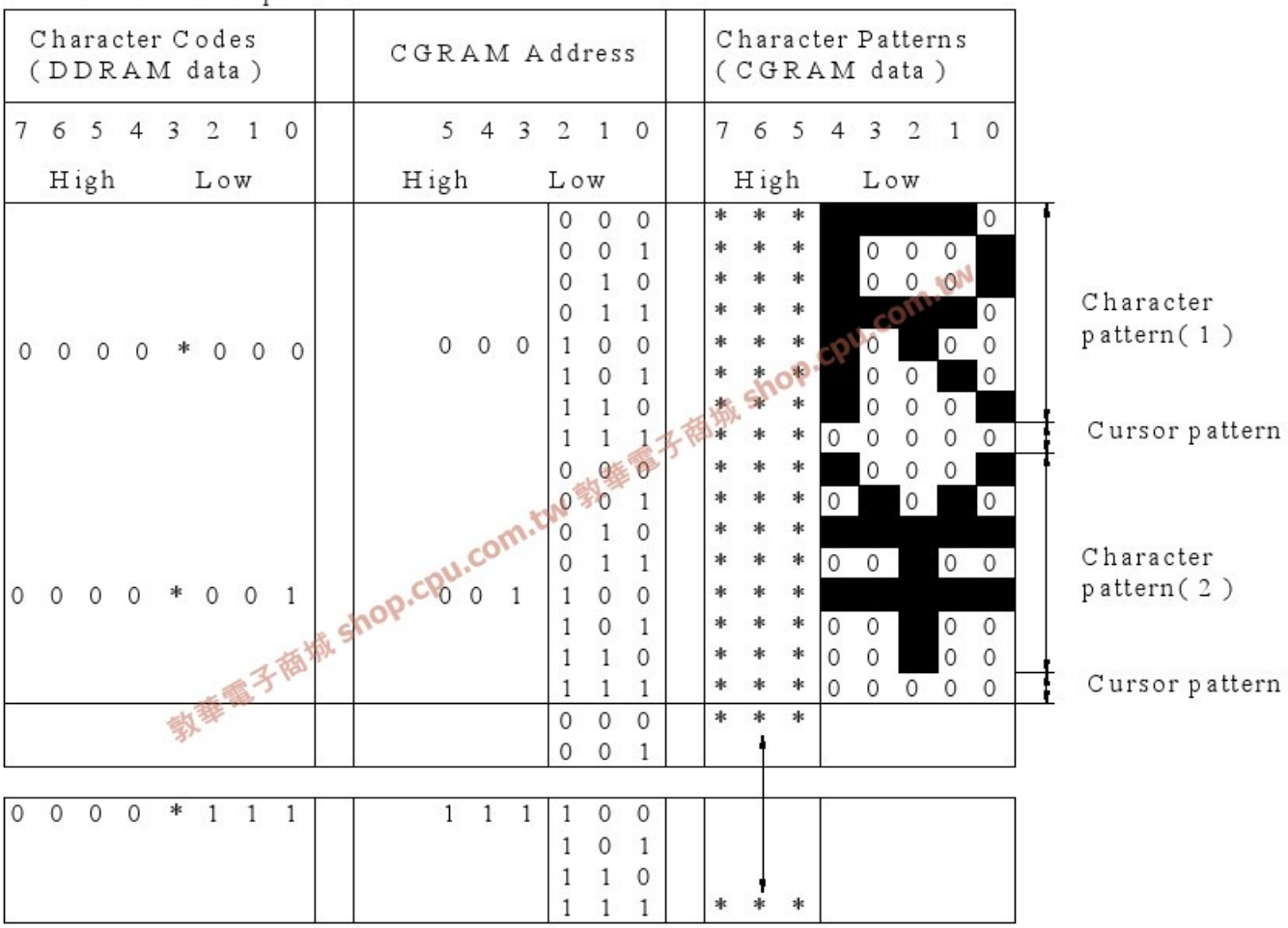
Character Generator RAM (CGRAM)

In CGRAM, the user can rewrite character by program. For 5×8 dots, eight character patterns can be written, and for 5×10 dots, four character patterns can be written.

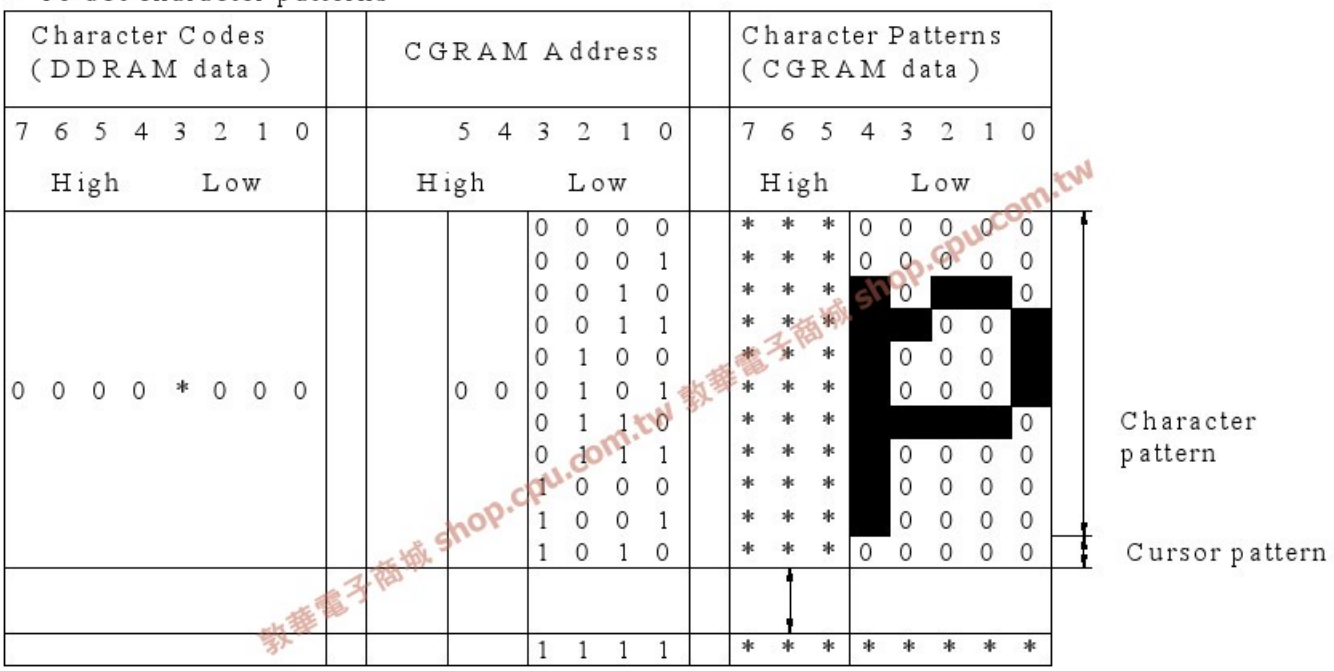
Write into DDRAM the character code at the addresses shown as the left column of table 1. To show the character patterns stored in CGRAM.

Relationship between CGRAM Addresses, Character Codes (DDRAM) and Character Patterns (CGRAM Data)

For 5 * 8 dot character patterns



For 5 * 10 dot character patterns



■ : " High "

※C.G ROM table.　English-Jopanese

Upper 4 bit / Lower 4 bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)															
LLLH	(2)															
LLHL	(3)															
LLHH	(4)															
LHLL	(5)															
LHLH	(6)															
LHHL	(7)															
LHHH	(8)															
HLLL	(1)															
HLLH	(2)															
HLHL	(3)															
HLHH	(4)															
HHLL	(5)															
HHLH	(6)															
HHHL	(7)															
HHHH	(8)															

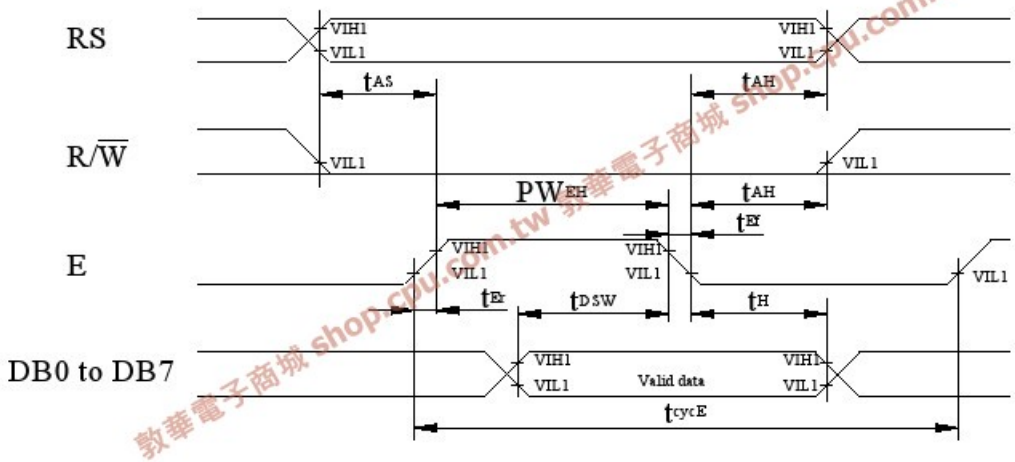
※. Instruction table

Instruction	Instruction Code										Description	Execution time
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "00H" to DDRAM and set DDRAM address to "00H" from AC	1.53ms
Return Home	0	0	0	0	0	0	0	0	1	—	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.53ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction and enable the shift of entire display.	39 μ s
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor (C), and blinking of cursor (B) on/off control bit.	39 μ s
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	—	—	Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data.	39 μ s
Function Set	0	0	0	0	1	DL	N	F	—	—	Set interface data length (DL:8-bit/4-bit), numbers of display line (N:2-line/1-line)and, display font type (F:5×11 dots/5× 8 dots)	39 μ s
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	39 μ s
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.	39 μ s
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0 μ s
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	43 μ s
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	43 μ s

—" : don't care

※ Timing characteristics

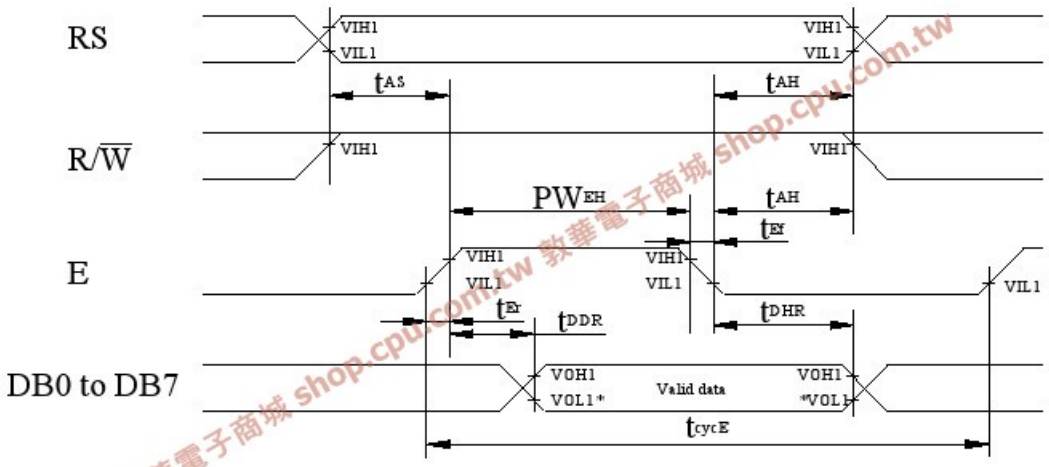
Write Operation



Ta=25℃,Vdd=5.0±0.5V

Item	Symbol	Min	Typ	Max	Unit
Enable cycle time	t_{cycE}	500	—	—	ns
Enable pulse width (high level)	PW_{EH}	230	—	—	ns
Enable rise/fall time	t_{Er},t_{Ef}	—	—	20	ns
Address set-up time (RS, R/W to E)	t_{AS}	40	—	—	ns
Address hold time	t_{AH}	10	—	—	ns
Data set-up time	t_{DSW}	80	—	—	ns
Data hold time	t_H	10	—	—	ns

Read Operation



NOTE: *VOL1 is assumed to be 0.8V at 2 MHZ operation.

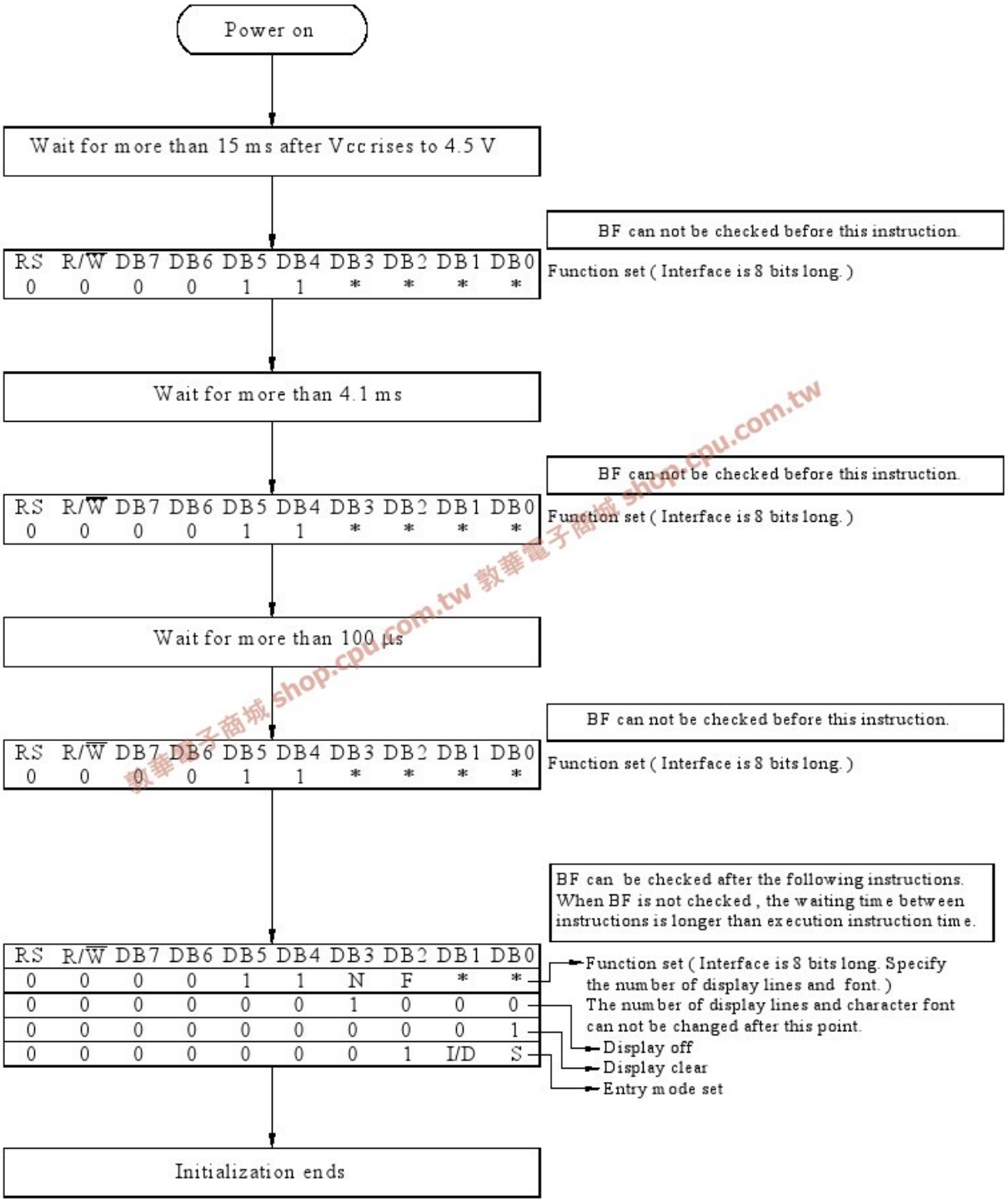
Ta=25℃,Vdd=5.0±0.5V

Item	Symbol	Min	Typ	Max	Unit
Enable cycle time	t_{cycE}	500	—	—	ns
Enable pulse width (high level)	PW_{EH}	230	—	—	ns
Enable rise/fall time	t_{Er},t_{Ef}	—	—	20	ns
Address set-up time (RS, R/W to E)	t_{AS}	40	—	—	ns
Address hold time	t_{AH}	10	—	—	ns
Data delay time	t_{DDR}	—	—	160	ns
Data hold time	t_{DHR}	5	—	—	ns

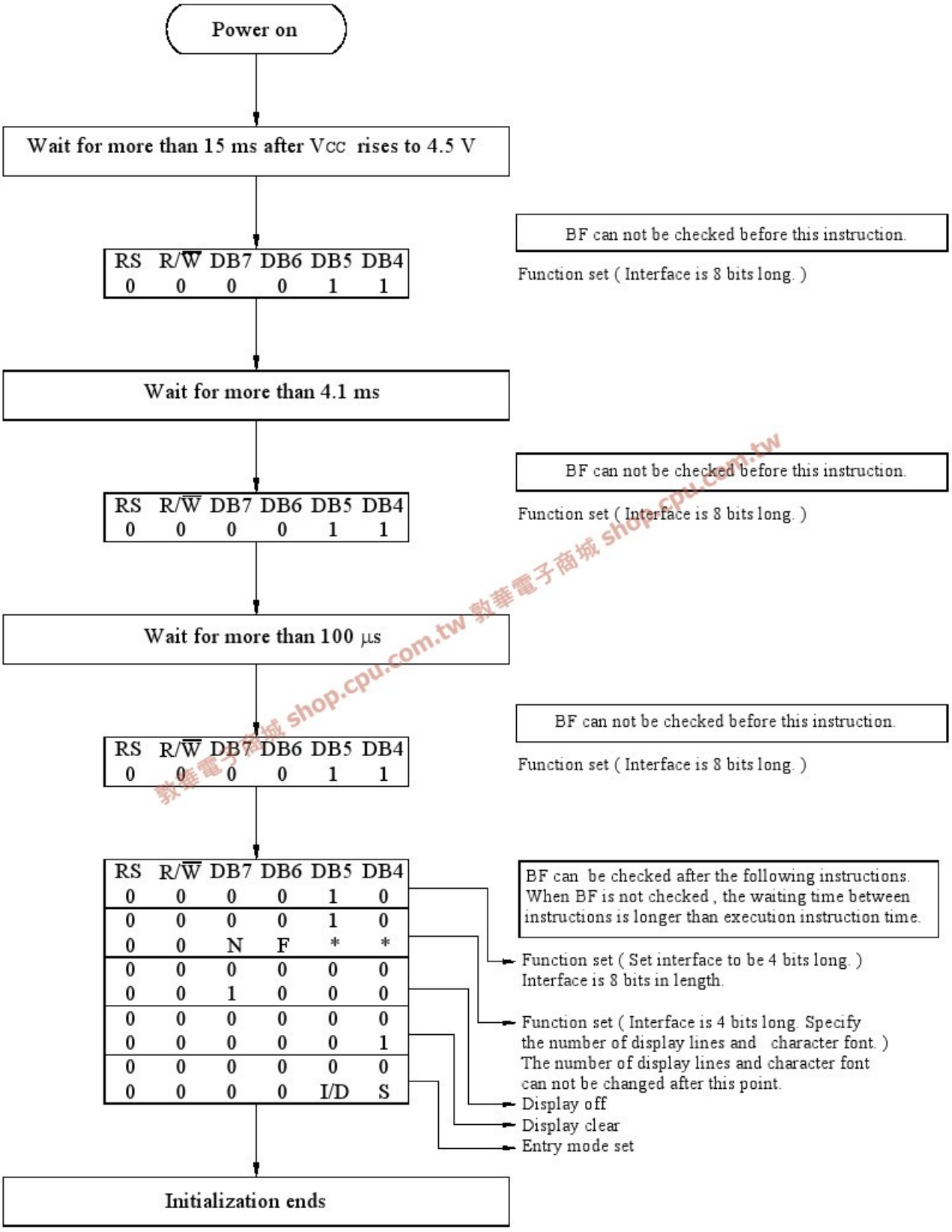
※ Initializing soft ware of LCM

8-bit interface

4-bit interface



8-Bit Ineterface



4-Bit Ineterface